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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/559,835	04/26/2000	Richard M. Barth	RA019C3DR	3026

7590 04/05/2002

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EXAMINER
NGUYEN, HIEP T

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 04/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

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EXAMINER
NGUYEN, HIEP T

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 02/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/559,835	Applicant(s) BARTH, ET AL.	
	Examiner Hiep T Nguyen	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-11* is/are allowed.

6)☒ Claim(s) *12-23 and 26-39* is/are rejected.

7)☒ Claim(s) *24,25,40 and 41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-41 are pending in the application.

2. Claims 15, 19-20, 29, and 35-36 rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

   2.1. For claims 15 and 29: the claimed limitation of "wherein the first column address and the first row address are both included in a first packet, and the second column address and the page mode information is included in a second packet" is not supported by the original disclosure.

   2.2. As per claims 19 and 35: the original disclosure does not support the claimed limitation of "wherein the first column address is received during a first clock cycle and the first row address is received during a second clock cycle". There is no disclosure of the relationship between the clock cycles and the bus cycles [e.g., bus cycles in figures 3 and 4].

   2.3. As per claims 20 and 36: the original disclosure does not support the claimed limitation of "a first portion of the first column address is received during a first bus cycle and a second portion of the first column address is received during a second bus cycle, and wherein both the first and the second bus cycles transpire during the first clock cycle".

3. Claims 12 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakui et al., U.S. Patent No. 5,173,878.

   3.1. As per claim 12: Sakui et al. teach a method of operation in a memory device, the memory device having an array of memory cells [figure 1], the method comprising:

      3.1.1. Receiving a first column address [see figure 2D], the first column address representing a column locality of a first storage location within a first row in the array;

      3.1.2. Receiving a first row address in succession to receiving the first column address [see figure 2C, and also col. 5, lines 54-62], the first row address representing a location of the first row in the array; and

3.1.3. Accessing [during the write cycle] a first memory cell of he array of memory cells, the first memory cell being located at the first storage location [see again col. 5, lines 54-62].

3.2. As per claim 26: Sakui teaches the claimed method through the write operation as mentioned in the rejection of claim 12. During the write operation, the system activates the CAS before the RAS. Thus, allowing the column address to be submitted to the memory (60) prior to the row address. Accordingly, each of the claimed steps "issuing a first column address to the memory device, the first column address representing a column locality of a first storage location within a first row in the array; and issuing a first row address following the issuance of the first column address, the first row address representing a location of the first row in the array" are taught.

HW 2/20/02

4. Claims 12-14, ~~16-16~~ 16-18, 21-23, 26-28, 30-34, and 37-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Farmwald et al., U.S. Patent No. 5,243,703.

4.1. As per claims 12 and 26: Farmwald et al. teach the claimed methods though a regular memory access cycle. In that access cycle, the column address [i.e., bits 0-8; figure 4; since DRAMs use lower bits for column addresses] is issued by the CPU or received by a memory [e.g., DRAM] through the second word [i.e., word 1] of the packet before issuing by the CPU or receiving by the memory a corresponding row address [i.e., bits 9-17 in word 2 of the packet; see figure 4; col. 10, lines 31-46]. Accordingly, Farmwald et al teach each of the claimed steps of claim 12 and 26.

4.2. As per claims 13 and 27: Farmwald further teach that the access type information including page mode information is also transmitted to the memory through word 0 of the request packet [see figure 4; col. 12, lines 34-51]. Furthermore, during a page mode access of a DRAM page, the row address remains the same; only new column addresses are needed for the remaining memory locations of the same page. Accordingly, each of the further claimed limitations are also taught by Farmwald et al.

4.3. As per claims 14 and 28: DRAMs such as that of Farmwald are accessed using row and column addresses. Furthermore, the same memory location and/or row of the DRAM must have been accessed by a requesting device [e.g., CPU] more than one during the entire lifetime of the

coupled memory device. Accordingly, Farnwald et al. inherently teach the further claimed limitation of "receiving a second row address in succession to receiving the second column address, the second row address representing the location of the first row in the array".

4.4. As per claims 16 and 30: the further claimed limitation of "wherein the first column address is received in a first portion of a request packet and the first row address is received in a second portion of the packet" is also taught by Farnwald et al. [see figure 4]. There are four and half words of the request packet containing addresses, wherein word 1 contains column address [since DRAMs use lower bits for column address, as mentioned].

4.5. As per claims 17 and 31: Farnwald further teaches the claimed limitation of "wherein the packet further includes start information representing the beginning of the packet". See bit (23) of figure 4, and col. 10, lines 36-38.

4.6. As per claims 18 and 32: the further claimed limitation of "receiving block size information, the block size information representing an amount of data to be output by the memory device" is also taught by Farnwald. See figure 4; word 5 of the request packet; col. 10, 45-46.

4.7. As per claim 21, 23, 37, and 39: Farnwald further teaches the claimed limitation of "receiving page mode access information". See col. 12, lines 34-53.

4.8. As per claims 22 and 38: Farnwald teaches that the page mode information and the first column address are sent by the CPU and received by the memory in the same request packet. Accordingly, the page mode information and the first column address are concurrently received by the memory in term of the time interval of receiving the request packet.

4.9. As per claims 33 and 34: as shown in figure 4, Farnwald's first column address, first row address and the block size information are included in the same packet.

5. Claims 24 and 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The claims are allowed over the prior art of record because none of the prior art of record teach or fairly suggests the further claimed limitation of "wherein the page mode access information includes a first portion and a second portion, wherein the first portion is received

concurrently with the first column address, and the second portion is received concurrently with the first row address." Accordingly, claims 25 and 41 would also be allowed over the prior art of record since claims 25 and 41 are depended on claims 24 and 40, respectively.

6. Claims 1-11 are allowed over the prior art of record for the same reason as set forth in paper no. 13, mailed June 11, 1997 of the parent application [08/784,464]. More specifically, the claims are allowed over the prior art of record because none of the prior art of record teaches or fairly suggests a method of transferring a packet of data first transmitting start information, lower order memory address bits, and first op code information in a first word and then transmitting second and third op code information and upper order memory address bits in a second word wherein these components are transmitted over specific buses and lines the bus as in claim 1, for example.
7. The original patent, or a statement as to loss or inaccessibility of the original patent, must be received before this reissue application can be allowed. See 37 CFR 1.178.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep T Nguyen whose telephone number is (703) 305-3822. The examiner can normally be reached on Monday-Friday from 9:30 a.m. to 6:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do H. Yoo can be reached on (703) 308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9600.

Hiep T. Nguyen

Hiep T Nguyen
Primary Examiner
Art Unit 2187